SEMICONDUCTOR DEVICE WITH INTEGRATED BREAKDOWN PROTECTION

FIELD OF INVENTION

[0001] The present embodiments relate to semiconductor devices.

BACKGROUND

[0002] Integrated circuits (ICs) and other electronic devices often include arrangements of interconnected field effect transistors (FETs), also called metal-oxide-semiconductor field effect transistors (MOSFETs), or simply MOS transistors or devices. A typical MOS transistor includes a gate electrode as a control electrode and spaced apart source and drain electrodes. A control voltage applied to the gate electrode controls the flow of current through a controllable conductive channel between the source and drain electrodes.

[0003] Power transistor devices are designed to be tolerant of the high currents and voltages that are present in power applications such as motion control, air bag deployment, and automotive fuel injector drivers. One type of power MOS transistor is a laterally diffused metal-oxide-semiconductor (LDMOS) transistor. In an LDMOS device, a drift space is provided between the channel region and the drain region.

[0004] LDMOS devices may be designed to operate in a high-side configuration in which all of the device terminals are level shifted with respect to the substrate potential. Devices configured for high-side operation have been applied in power switchers in DC-to-DC converters, which have respective LDMOS devices for the high side and low side. High-side capable devices may be designed to prevent a direct punch-through path from a body region of the LDMOS device to an underlying substrate.

[0005] LDMOS devices are often used in applications, such as automotive applications, involving operational voltages greater than 45 Volts. Breakdown resulting from applying such high voltages to the drain is often prevented through a reduced surface field (RESURF) structure in the LDMOS device design. The RESURF structure is designed to deplete the drift space of the

[0006] LDMOS device in both vertical and lateral directions, thereby reducing the electric field near the surface at the drift region and thus raising the off-state breakdown voltage (BVdss) of the device.

[0007] Breakdown events may nonetheless occur at an intrinsic location along the current conduction path between the drain and source of an LDMOS device. Such intrinsic breakdown events often lead to device degradation or failure. One technique for avoiding intrinsic breakdown involves clamping the drain voltage with a second device in parallel with the LDMOS device. The drain voltage is clamped to a level between the expected operating voltage of the LDMOS device and the intrinsic breakdown voltage of the LDMOS device. The second device undesirably leads to additional fabrication costs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The components and the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. Moreover, in the figures, like reference numerals designate corresponding parts throughout the different views.

[0009] FIGS. **1-5** are cross-sectional, schematic views of exemplary n-channel LDMOS transistors with integrated breakdown protection diodes in accordance with several embodiments.

[0010] FIGS. **6-8** are cross-sectional, schematic views of exemplary n-channel LDMOS transistors with integrated breakdown protection diodes in accordance with several further embodiments.

[0011] FIGS. **9A-9C** are cross-sectional, schematic views of exemplary n-channel LDMOS transistors with integrated breakdown protection diodes in accordance with still further embodiments.

[0012] FIG. **10** is flow diagram of an exemplary fabrication sequence to construct an n-channel LDMOS transistor with an integrated breakdown protection diode in accordance with one embodiment.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

[0013] The disclosure relates to LDMOS and other power transistor devices and electronic apparatus configured with one or more integrated breakdown protection diodes. Each protection diode may include or correspond with a junction having a breakdown voltage configured to protect a channel or other conduction region or path of the device. Each protection diode may be electrically tied or clamped to the power transistor device (e.g., in a parallel configuration) to experience the voltage applied to the terminals of the power transistor device. The junction of the protection diode is configured to breakdown at a voltage level lower than a breakdown voltage of the power transistor device near the conduction path. Breakdown protection is thus provided by relocating the site of the breakdown event rather than by trying to prevent breakdown from occurring altogether. The relocation moves the breakdown site from the conduction path to the location of the diode or junction. As described below in connection with several examples, the protection diode or junction is not disposed in (e.g., is spaced from) a normal conduction path of the device. A breakdown event (e.g., an electrostatic discharge (ESD) event) occurring at such diodes or junctions is thus non-destructive to normal device operation, as described below.

[0014] The protection diode or junction may nonetheless be internal or integrated into an interior or active area of the device. In such cases, the protection diode is not disposed in, for example, an end termination region of the device. The internal nature and/or other aspects of the integration may allow the protection diode to scale with device size (e.g., transistor width). The internal nature of the integration may also allow the breakdown protection to be provided without requiring an increase in device footprint or overall size.

[0015] The integration may be achieved in some embodiments without adding fabrication steps to the fabrication process. In some embodiments, the integration of the protection diode is achieved via a modification to a pre-existing mask layout. For example, the protection diode may be formed via a layout change in a pre-existing implantation step directed to forming an isolating region or a body region of the device. The pre-existing implantation step may alternatively be directed to the formation of a logic device (e.g., a CMOS transistor). In some embodiments, a separate implant or other formation fabrication step may thus be avoided.

[0016] The protection diode or junction may be integrated with one or more isolating regions of the LDMOS or other